Q2

35. (Amended) The method as claimed in claim 33, further comprising a step of biasing the n-type MOS transistor to trigger the rectifier.

REMARKS

In the present Amendment, Applicants have amended claims 32, 34, and 35 to correct some typographical errors. No new matter has been added.

In the Office Action, the Examiner rejected claims 1-17 and 33 under 35 U.S.C. §103(a) as being unpatentable over Ker et al. (U.S. Patent Publication 2002/0084490, referred to as Ker et al.(1) hereinafter) in view of Zhang et al. (U.S. Patent No. 5,824,573), and rejected claims 18-32 and 34-35 under 35 U.S.C. §103(a) as being unpatentable over Ker et al.(1) in view of Zhang et al., and further in view of Ker et al. (U.S. Patent No. 5,631,793, referred to as Ker et al.(2) hereinafter).

Applicants respectfully traverse the rejections under 35 U.S.C. §103(a) because a *prima facie* case of obviousness has not been established by the Examiner.

The present invention is in general directed to an electrostatic discharge (ESD) protection circuit incorporating a silicon controlled rectifier (SCR) in a silicon-on-insulator (SOI) semiconductor device. Particularly, claim 1 recites, among others, "a layer of silicon material, formed over the isolation layer, including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, a second n-type portion contiguous with the second p-type portion, a third p-type portion contiguous with the second n-type portion, and a third n-type portion contiguous with the third p-type portion".

Ker et al.(1), co-invented by one of the co-inventors of the present invention, describes PMOS-bound and NMOS-bound diodes for ESD protection and the application circuits thereof. The PMOS-bound or NMOS-bound diode comprises a first

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

semiconductor layer of a first conductivity type and a MOS transistor of a second conductivity type. The MOS transistor has a circular gate, a drain diffusion region and a gate diffusion region. Both of the drain and gate diffusion regions are of the second conductivity type.

Zhang et al. describes a manufacturing method of a semiconductor device, wherein nickel is introduced to an amorphous silicon film to crystallize the amorphous silicon film. After forming gate electrodes and others, a source, a drain, and a channel are formed by doping impurities and laser irradiated to improve the crystallization of the amorphous silicon film.

Ker et al.(2), also co-invented by one of the co-inventors of the present invention, describes a capacitor-couple ESD protection circuit. The ESD protection circuit includes an ESD bypass device for bypassing an ESD current, a capacitor-couple circuit, and a potential leveling device.

To establish a *prima facie* case of obviousness under 35 U.S.C. §103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. (See M.P.E.P. §2143.03 (8th ed. 2001).) Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." (M.P.E.P. §2143 (8th ed. 2001).)

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

First, Applicants respectfully submit that Ker et al.(1)'s disclosure is clearly different from the field of the present invention, because Ker et al.(1) describes a device structure based on conventional MOS technologies, while the present invention is directed to SOI technologies. For example, claim 1 recites, among others, "an isolation layer formed over the semiconductor substrate . . . [and] a layer of silicon material, formed over the isolation layer". There is no disclosure or suggestion whatsoever in Ker et al.(1) of these features recited in claim 1 or of anything related to SOI technologies. Therefore, one skilled in the art would not be motivated to apply Ker et al.(1)'s teachings to or combine Ker et al.(1) with any reference in practicing the present invention.

In rejecting claim 1, the Examiner alleged that "Ker et al.[(1)] teaches all of the claimed matter in claim 1 except for the rectifier consisting of a CMOS circuit . . . but instead teaches it as separate NMOS and PMOS circuitry". Applicants respectfully disagree with this statement.

As discussed above, Ker et al.(1) at least fails to teach the "isolation layer" and "the rectifier consisting of a CMOS circuit", as recited in claim 1. Furthermore, claim 1 recites, among others, "a layer of silicon material, . . . , including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, a second n-type portion contiguous with the second p-type portion, a third p-type portion contiguous with the second n-type portion, and a third n-type portion contiguous with the third p-type portion, wherein the first, second, and third p-type portions and the first, second, and third n-type portions collectively form a rectifier". According to the Examiner, Ker et al.(1)'s elements 44, 46b, and 52 of Fig. 9 and elements 42, 44b, and 46 of Fig. 7 correspond to Applicants'

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

claimed first p-type portion, first n-type portion, second p-type portion, second n-type portion, third p-type portion, and third n-type portion, and "wherein the first, second , and third p-type portions and the first, second, and third n-type portions collectively form a rectifier (Ker et al.(1) (PMOS) *Figure 7 . . . & Figure 9 . . .*)" (Office Action, page 3). Applicants respectfully submit that, **because Figure 7 and Figure 9 of Ker et al.(1) illustrate two separate devices**, *(a)* element 42 of Fig. 7, allegedly corresponding to Applicants' claimed second n-type portion, cannot be contiguous with element 52 of Fig. 9, allegedly corresponding to Applicants' claimed second p-type portion; and *(b)* elements 44, 46b, and 52 of Fig. 9 and elements 42, 44b, and 46 of Fig. 7 cannot **"collectively"** form a rectifier. As a result, Ker et al.(1) at least fails to teach the features of "an isolation layer", "a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, a second n-type portion contiguous with the second p-type portion, a third p-type portion contiguous with the second n-type portion, and a third n-type portion contiguous with the third p-type portion", and "the first, second, and third p-type portions and the first, second, and third n-type portions collectively [forming] a rectifier".

With regard to Zhang et al., the Examiner alleged that channel region 112 of Fig. 2C corresponds to Applicants' claimed third p-type portion and channel region 115 corresponds to Applicants' claimed first n-type portion as recited in claim 1. Applicants note that, Zhang et al. requires "an intrinsic ([i] type[)] amorphous silicon film 104 . . . deposited by a plasma CVD method." (Col. 8, lines 30-33.) Following the processing steps, see col. 8, line 30 to col. 10, line 28, it is clear that channel regions 112 and 115 are part of amorphous silicon film 104, and therefore are intrinsic, contrary to what is

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

recited in claim 1. Thus, Zhang et al. fails to teach or suggest the "third p-type portion" and the "first n-type portion" of claim 1, and therefore fails to teach or suggest the recited features of claim 1. The requirement of Zhang et al. that channel regions 112 and 115 be intrinsic actually teaches away from the present invention.

Therefore, Ker et al.(1) and Zhang et al., taken alone or combined, fail to teach or suggest "each and every element" of the present invention as recited in claim 1.

Applicants submit that, in addition to the above rationale, there is no motivation to combine Ker et al.(1) and Zhang et al. According to the Examiner, Zhang et al.'s element 112 of Fig. 2D corresponds to Ker et al.(1)'s element 44b of Fig. 7, while Zhang et al.'s element 115 of Fig. 2D corresponds to Ker et al.(1)'s element 46b of Fig. 9 (Office Action, pages 2-3). Applicants note that, elements 112 and 115 of Zhang et al.'s disclosure are the channel regions of PTFT and NTFT, respectively (Zhang et al., col. 10, lines 24-28), while elements 44b of Fig. 7 and 46b of Fig. 9 of Ker et al.(1) correspond to one of the drain and source regions of the PMOS and NMOS transistors, respectively. Moreover, claim 1 of Ker et al.(1) describes "a MOS transistor . . . comprising . . . a circular gate . . . and a second source/drain diffusion . . . enclosing the circular gate", while Zhang et al. describes gates 107 and 109 as being stripes of layers, as shown in Fig. 3. Therefore, there is no indication of any likelihood of success by applying Zhang et al.'s teachings with those of Ker et al.(1).

In view of the above, Ker et al.(1) and Zhang et al., taken alone or combined, fail to teach or suggest each and every element of the present invention, nor would one skilled in the art be motivated to combine Zhang et al.'s teachings with Ker et al.(1)'s teachings to result in the present invention, and neither would there be any reasonable

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

expectation of success in doing so, in view of such teaching-away references. As a result, Applicants respectfully request that the rejection of claim 1 under 35 U.S.C. §103(a) be withdrawn, placing claim 1 in an allowable condition.

Claims 2-16, which directly or indirectly depend from claim 1, are therefore also allowable at least because of their dependencies from an allowable base claim.

Regarding the rejection of independent claim 17 under 35 U.S.C. §103(a), Applicants respectfully submit that, for the foregoing reasons, Ker et al.(1) fails to teach or suggest each and every element of the present invention as recited in claim 17. Particularly, Ker et al.(1) fails to teach the recited features of "an n-type MOS transistor . . . ***and*** a p-type MOS transistor" (emphasis added), "the n-type MOS transistor and the p-type MOS transistor [forming] a rectifier to provide electrostatic discharge protection".

Zhang et al., as already discussed, fails to teach or suggest every feature of claim 17 of the present invention. Zhang et al. only describes an active matrix type liquid crystal display composed of thin film transistors (TFT), and the manufacturing method thereof. Assuming that, *arguendo*, according to the Examiner, the TFTs of Zhang et al. correspond to Applicants' claimed MOS transistors, Zhang et al. still fails to teach "the n-type MOS transistor and the p-type MOS transistor [forming] a rectifier to provide electrostatic discharge protection". Therefore, Zhang et al. does not overcome the above-mentioned deficiencies of Ker et al.(1). In other words, Ker et al.(1) and Zhang et al., taken alone or combined, fail to teach each and every element of the present invention as claimed in claim 17.

Similarly, regarding the rejection of independent claim 33 under 35 U.S.C. §103(a), Applicants submit that, for the reasons already discussed, Ker et al.(1) does

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

not teach or suggest at least the features of "providing an n-type MOS transistor . . . [and] providing a p-type MOS transistor", "providing a p-type region contiguous with one of the source region and the drain region of the n-type MOS transistor to form a cathode", "providing a p-type region contiguous with one of the source region and the drain region of the n-type MOS transistor to form an anode", and "wherein the n-type region, the p-type region, the p-type MOS transistor and the n-type MOS transistor form a rectifier". Zhang et al. does not overcome these deficiencies.

Additionally, for the same arguments in traversing the rejection of claims 1-16, there is no motivation to Ker et al.(1) with Zhang et al., nor is there any reasonable expectation of success in doing so.

As a result, Applicants submit that claims 17 and 33 are allowable under 35 U.S.C. §103(a), and request that the rejection of claims 17 and 33 be withdrawn.

Claims 18-32 and 34-35, which directly or indirectly depend from claims 17 and 33, respectively, are therefore also allowable under 35 U.S.C. §103(a) at least because of their dependencies from an allowable base claim.

The Examiner further rejected claims 18-32 and 34-35 under 35 U.S.C. §103(a) as being unpatentable over Ker et al.(1), in view of Zhang et al., and further in view of Ker et al.(2). Applicants respectfully point out that, on page 9 of the Office Action, the Examiner appears to have erroneously corresponded Ker et al.(2)'s PMOS transistor Mp1 of Fig. 2 to both Applicants' claimed p-type MOS transistor and the first PMOS transistor. Assuming, according to the Examiner, Ker et al.(2)'s PMOS transistor Mp1 corresponds to Applicants' claimed first PMOS transistor, and NMOS transistor Mn1 corresponds to Applicants' claimed first NMOS transistor. However, Ker et al.(2) still

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

fails to teach or suggest at least "an n-type MOS transistor" and "a p-type MOS transistor . . . contiguous with the n-type MOS transistor". In addition, contrary to the Examiner's statements, Mp1 and Mn1 do ***not*** form an inverter, the gate of Mp1 is ***not*** coupled to the gate of Mn1, and, since Ker et al.(2) does not include the p-type MOS transistor, the gate of the p-type MOS transistor is ***not*** coupled to the drain regions of Mp1 and Mn1.

For the foregoing reasons, neither Zhang et al. nor Ker et al.(2) overcomes the described deficiencies of Ker et al.(1).

Accordingly, Applicants respectfully request that the rejection of claims 18-32 and 34-35 under 35 U.S.C. §103(a) be withdrawn, placing them in an allowable condition.

In view of the foregoing amendments and remarks, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of pending claims 1-35.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: March 18, 2003

By: Reg # 31,744
Yitai Hu
Reg. No. 40,653

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

APPENDIX TO THE AMENDMENT FILED ON MARCH 18, 2003

Amended claims:

32. (Amended) The integrated circuit device as claimed in claim [29] 31, wherein the cathode is coupled to at least one diode to prevent the rectifier from being triggered in a non-ESD operation.

34. (Amended) The method as claimed in claim [31] 33, further comprising a step of biasing the p-type MOS transistor to trigger the rectifier.

35. (Amended) The method as claimed in claim [31] 33, further comprising a step of biasing the n-type MOS transistor to trigger the rectifier.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com